REMARKS

This amendment is in response to the Official Action dated September 11, 2007. Claims 24, 31, 34, 36, and 41 have been amended; as such claims 24-44 remain pending in this application. Claims 24, 31, 34, 36, and 41 are independent claims. Reconsideration and allowance is requested in view of the claim amendments and the following remarks.

Rejections under 35 U.S.C. § 102

Claims 24, 25, 27, and 32 have been rejected under 35 U.S.C. § 102 as anticipated by U.S. Patent No. 6,539,511 to Hashizume.

Claim 24 recites:

> *A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising:*
> *a scan in terminal providing an inputted scan pattern to a scan chain between said scan in terminal and a scan out terminal;*
> *a plurality of flip-flops arranged in said scan chain so as to perform scan testing for said internal logical circuitry responsive to said scan pattern; and*
> *a reset means for resetting said plurality of flip-flops at a transition time, between said test mode and said normal mode, responsive to said scan mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal,*
> *whereby said resetting is always performed at said transition time.*

Hashizume fails to teach or suggest "*a reset means for resetting said plurality of flip-flops at a transition time, between said test mode and said normal mode, responsive to said scan mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal, whereby said resetting is always performed at said transition time.*"

Hashizume discloses a semiconductor integrated circuit capable of executing various types of boundary scan tests. Hashizume's invention executes an external test command which causes the BSR control circuit to perform a set or reset operation in a register chain.

In the seventeenth embodiment of the cited reference, Hashizume discloses that during the test mode the BSRs are provided with a set or reset instruction, causing the BSRs in the semiconductor integrated circuit to be set to either "0" or "1", respectively, at the same time in response to the external test command. The BSRs are either set or reset, during test mode, depending on the provided test mode instruction. While in the test mode, it is arbitrary (based on an external/user selection) whether the BSRs are set or reset. Therefore, even when a given BSR is reset, it is reset *during* test mode, not during the *transition* between test and normal mode.

By contrast, in claim 24, the test mode is a mode for performing a scan test, not for resetting the semiconductor integrated circuit during the test mode sequence. In the invention recited in claim 24, the circuit is *always* reset (compulsory reset) whenever the mode is *switched* between the normal mode and the test mode. In other words, the reset is not arbitrarily selected as part of the test mode process as a value to load into the registers (BSRs). Instead, the reset is always executed when *switching* between the normal mode and the test mode. As such, the reset is not performed *during* the test mode, but only occurs during the transition when the mode is *switched.*

In amended claim 24, the compulsory reset of the flip-flops is performed when the mode is switched from the normal mode to the test mode, making it possible to prevent the read function. This function, in which data in the normal mode is shifted out during test mode, distinguishes the claim from the conventional art.

The compulsory reset of the flip-flops is also performed at a timing when the mode is switched from the test mode to the normal mode, making it possible to prevent the following incidence from happening. The incidence is such that security data is outputted in a normal mode by setting certain conditions in a test mode. Such a function was allowed in the conventional art.

These above cited features allow the disclosed semiconductor integrated circuit to prevent unauthorized readout or rewriting of data stored within the LSI. The compulsory reset, during mode transitions, offers the benefit of actively, forcibly, preventing access to the data in the normal mode, while keeping the scan test functionality available.

As described above, in the cited art (Hashizume), external test commands in line with objects of arbitrary tests are freely set in a command register in order to achieve the object of Hashizume's invention, which is to allow execution of various tests as much as possible.

In contrast, the present invention is configured such that functions other than functions required for the scan test are controlled (limited or prevented) to achieve the object of maintaining securing as much as possible while keeping scan test function available.

In other words, the objects and configurations of the cited art and the present invention are clearly different from each other, and they are contradictory.

Accordingly, the present invention is not obvious at all in view of the cited art Hashizume which is based on the contradictory idea.

The cited art and the present invention are clearly different from each other. Therefore, Hashizume fails to teach or suggest various features of independent claim 24. Furthermore, at least for the reason disclosed above, claims 25, 27, and 32 overcome Hashizume because they depend on independent claim 24.

Accordingly, Applicant respectfully requests that the rejection of claims 24, 25, 27, and 32 under 35 U.S.C. § 102 be withdrawn.

Rejections under 35 U.S.C. § 103

Claims 26, 31, 34, 36, and 37 have been rejected under 35 U.S.C. § 103 as being unpatentable over Hashizume in view of Cavaliere et al. (U.S. Patent No. 3,961,254); Claims 28, 29, 33, 41, 43, and 44 have been rejected under 35 U.S.C. § 103 as being unpatentable over Hashizume in view of Tamamura et al. (U.S. Patent No. 6,118,316).

Claim 31 recites:

> *A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising:*
> *a plurality of flip-flops arranged so as to perform scan testing for said internal logical circuitry;*
> *memory means connected to said plurality of flip-flops; and*
> *access control means for prohibiting access to said memory means during said test mode, the prohibiting being switched at a transition time between said test mode and said normal mode in accordance with a mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal,*
> *whereby said prohibiting is always performed during said test mode.*

In claim 31, the compulsory prohibition of access to the plurality of flip-flops during the test mode can forcibly limit (prevent) the ability to read/write to memory during test mode. As such, access to test mode data is prevented, while keeping the scan test function available.

As described above, the object of the invention disclosed by Hashizume is to enable execution of various types of boundary scan tests on a semiconductor integrated circuit. To do this, Hashizume's invention executes an external test command which causes the BSR control circuit to perform a set or reset operation on the register chain.

By contrast, claim 31 discloses that functions (other than functions required to initiate the scan test) are secure from access during the test mode. Access to the memory means is always prohibited (compulsory prohibition) during the test mode. The access prohibition is not arbitrary.

Whenever the device is placed in the test mode, the access will be prohibited, at which point no test data is readable from the semiconductor integrated circuit.

Claim 36 recites, in part:

> *a reset means for resetting said plurality of flip-flops at a transition time, between said test mode and said normal mode, responsive to said scan mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal,*
> *wherein said reset means is responsive to a reset signal inputted from a reset input terminal and resets said plurality of flip-flops at said transition time, between said test mode and said normal mode, in accordance with said mode signal…*
> *whereby said resetting is always performed at said transition time.*

Hashizume fails to teach or suggest "*a reset means for resetting said plurality of flip-flops at a transition time, between said test mode and said normal mode … whereby said resetting is always performed at said transition time.*"

As set forth above, Hashizume discloses that during the test mode the BSRs are provided with set and reset instruction, causing the BSRs in the semiconductor integrated circuit to be set to either "0" or "1", respectively, at the same time in response to the external test command. However, even when a given BSR is reset, it is reset *during* test mode, not during the *transition* between test and normal mode.

By contrast, in claim 36, the test mode is a mode for performing a scan test. Not for resetting the semiconductor integrated circuit as a part of the test mode sequence. In the invention recited in Claim 36, the circuit is *always* reset (compulsory reset) whenever the mode is *switched* between the test mode and the normal mode.

This function, in which data from the test mode is shifted out when normal mode is initiated, distinguishes the claim from the conventional art.

These above cited features allow the disclosed semiconductor integrated circuit to prevent unauthorized readout or rewriting of security data stored within the LSI. The compulsory reset, during mode transitions, offers the benefit of actively, forcibly, preventing access to secure information, while keeping the scan test functionality available.

Cavaliere discloses an LSI semiconductor device, including circuitry for testing embedded memory arrays. Cavaliere does not disclose a technique for prohibiting normal mode output, while supplying test mode data.

Tamamura discloses a semiconductor integrated circuit for generating a stabilized oscillation signal based on an input signal. Even a cursory review of Tamamura shows that Tamamura fails to disclose a technique for prohibiting normal mode output while supplying test mode data.

Neither Cavaliere nor Tamamura, either alone or in any proper combination, cure the deficiencies of Hashizume with respect to at least the previously identified features of claims 31 and 36. Therefore, Applicant submits that a prima facie case of obviousness for claims 31 and 36 has not been presented.

For the reasons stated above, claims 34 and 41 also overcome Hashizume, Cavaliere, and Tamamura. Furthermore, at least for the reason disclosed above, claims 26, 28, 29, 33, 37, 43, and 44 overcome the combination of Hashisumze, Cavaliere and Tamamura because they depend on independent claims 31, 34, 36, and 41.

Accordingly, Applicant respectfully requests that the rejection of claims 26, 28, 29, 31, 33, 34, 36, 37, 41, 43, and 44 under 35 U.S.C. § 103(a) be withdrawn.

Claim 30 has been rejected under 35 U.S.C. § 103 as being unpatentable over Hashizume in view of Bae et al. (KR 200101164); Claim 35 has been rejected under 35 U.S.C. § 103 as being unpatentable over Hashizume in view of DeLisle et al.(U.S. Patent No. 5,283,889); Claims 38 and 39 have been rejected under 35 U.S.C. § 103 as being unpatentable over Hashizume in view of Cavaliere et al., in further view of Tamamura; Claim 40 has been rejected under 35 U.S.C. § 103 as

being unpatentable over Hashizume in view of Cavaliere, in further view of Bae et al.; Claim 42 has been rejected under 35 U.S.C. § 103 as being unpatentable over Hashizume in view of Cavaliere, in further view of DeLisle et al.(U.S. Patent No. 5,283,889).

As previously described, Hashizume does not disclose, teach, or suggest at least the features of "*a reset means for resetting said plurality of flip-flops at a transition time, between said test mode and said normal mode, responsive to said scan mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal, whereby said resetting is always performed at said transition time*," as recited in independent claim 24.

Similarly, Hashizume does not disclose, teach, or suggest at least the features of "*access control means for prohibiting access to said memory means during said test mode, the prohibiting being switched at a transition time between said test mode and said normal mode in accordance with a mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal whereby said prohibiting is always performed during said test mode*," as recited in independent claim 31.

Independent claims 34, and 41also include similar subject matter to claims 24, 31 and 36, not found in Hashizume. Furthermore, dependent claims 25-30, 32-33, 35, 37-40, and 42-44 depend on the independent claims and therefore include the features of the independent claims not found in Hashizume.

DeLisle discloses an integrated circuit having a reset signal, but not a testing mode. DeLisle fails to disclose a technique for prohibiting normal mode output while supplying testmode data.

Bae discloses a clock generating apparatus capable of generating test pulses synchronized with another clock signal. However, Bae fails to disclose a technique for prohibiting normal mode output, while supplying testmode data.

Even assuming, arguendo, that Hashizume, Cavaliere, Tamamura, and Bae were combinable (which Applicant does not admit), Applicant submits that none of the cited references of Cavaliere,

Tamamura, and Bae, either alone or in any proper combination, cure the deficiencies of Hashizume with respect to at least the previously identified features of claim 24, 31, 34, 36, and 41. Furthermore, at least for the reason disclosed above, 25-30, 32-33, 35, 37-40, and 42-44 also overcome the combination of Hashizume, Cavaliere, Tamamura, and Bae because they depend on the independent claims.

Therefore, Applicant respectfully requests that the rejection of claims 26, 28-31, and 33-44 under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 18-0013, under Order No. SON-2810 from which the undersigned is authorized to draw.

Dated: February 25, 2008

Respectfully submitted,

By _____ 40,290

Ronald P. Kananen
Registration No.: 24,104
Christopher M. Tobin
Registration No.: 40,290
RADER, FISHMAN & GRAUER PLLC
Correspondence Customer Number: 23353
Attorneys for Applicant